UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,617	01/26/2004	Edward R. Rhoads	ITL.0241D1US (P7376D)	8924

21906 7590 07/26/2007

TROP PRUNER & HU, PC
1616 S. VOSS ROAD, SUITE 750
HOUSTON, TX 77057-2631

EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
07/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/764,617
Filing Date: January 26, 2004
Appellant(s): RHOADS ET AL.

Timothy N. Trop
(Reg. No. 28,994)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/11/2007 appealing from the Office action mailed 12/28/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,948,099	TALLAM	9-2005
5,594,903	BUNNELL ET AL.	1-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-15 and 26-30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,948,099. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the claimed features of he present Application serial No. 10/764,617 are transparently found in U.S. Patent no. 6,948,099. Take an example of independent claim 10 of the present Application and independent claim 2 of the U.S. Patent as following table:

Application Serial No. 10/764,617	U.S. Patent No. 6,948,099
A non-volatile, reprogrammable semiconductor memory comprising:	A memory comprising:
a plurality of addressable partitions, including a partition storing an operating system, and	a first portion storing a primary operation system;
a storing location storing an address for one of said partitions in association with information about the information stored in said partition.	a second portion storing a recovery operating system and instructions adapted to obtain a new operating system from outside said memory; and
	wherein said memory is a FLASH memory.

According to the example in the table above, the differences between the current application (10/764,617), and the US Patent (6,948,099) is the US Patent further defined a second portion storing a recovery operation system and instructions, and the memory is a Flash memory, It is obviousness to a person of ordinary skill in the art at the time the invention was made to recognize a non-volatile, reprogrammable semiconductor memory in the current application is same type as Flash memory, i.e., non-volatile memory, and the instructions stored in the second portion as defined in the US Patent (6,948,099) is an address stored in the partition as defined in the current application (10/764,617). Thus, claims 1-15 and 26-30 in current application (10/764,617) are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No. 6,948,099.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-15 and 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Tallam (US PAT. 6,948,099).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the

inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Tallam discloses a method of organizing stored information on a non-volatile, reprogrammable semiconductor memory (14, figure 1 and col. 2 lines 28-44) comprising partitioning said memory into a plurality of partitions (20 and 22, figure 2 and col. 2 line 66 through col. 3 line 15), each having a defined address (col. 2 line 45 through col. 3 line 15), and storing the defined address for one partition in another partition (col. 2 line 66 through col. 4 line 6).

Regarding claim 2, Tallam discloses the method further including storing information about the number of partitions (col. 4 line 59 through col. 5 line 39).

Regarding claims 3-5, Tallam discloses the method further including storing a boot loader (102, figure 5), a file system (106, figure 5), and a kernel for an operating system (104, figure 5) in one of said partition (col. 4 line 59 through col. 5 line 18).

Regarding claim 6, Tallam discloses the method further including storing information in association with the addresses about whether or not an integrity check needs to be done on the data stored at association address (col. 4 lines 26-50).

Regarding claims 7-9, Tallam discloses the method further including storing, in association with the address of a partition, information about the type of information stored in the partition, and storing information about whether or not the information stored at given partition is a boot loader, a kernel or a file system, and storing information about the load address for said information in association with said address (col. 4 line 59 through col. 5 line 38, figure 5).

Regarding claim 10, Tallam discloses a non-volatile, re-programmable semiconductor memory (14, figure 1 and col. 2 lines 36-44), comprising a plurality of addressable partitions, (20 and 22, figure 14), including a partition storing an operating system, i.e., primary operation system (22, figure 2), a storage location storing an address for one of said partitions in association with information about the information stored in said partition (20, figure 3, and col. 3 line 16 through col. 4 line 25).

Regarding claim 11, Tallam discloses a non-volatile, re-programmable semiconductor memory is a FLASH memory (col. 2 lines 36-44).

Regarding claims 12-25, Tallam discloses a non-volatile, re-programmable semiconductor memory wherein one of the said partitions stores a basic input/output system (32, figure 3), a file system (106, figure 5), a kernel for an operating system (104, figure 5), and a boot loader (102, figure 5).

Regarding claim 26, Tallam discloses a processor-based system (12, figure 6) comprising a processor (65, figure 6), a volatile memory (68, figure 6) coupled to said processor, and a re-programmable, non-volatile semiconductor memory (14 figure 6) coupled to said processor (col. 5 line 43 through col. 6 line 24), the semiconductor memory including a plurality of partitions (20 and 22, figure 2), one of said partitions storing an operating system (22, figure 2), and another of said partitions storing the address of the other partitions in association with information about what is stored in each of the partitions (figure 5 and col. 4 line 59 through col. 5 line 38).

Regarding claim 27, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claims 28-30, the limitations of the claims are rejected as the same reasons set forth in claims 12-25.

5. Claims 1-15 and 26-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bunnell et al. (US Pat. 5,594,903 hereinafter Bunnell).

Regarding claim 1, Bunnell discloses a method of organizing stored information on a non-volatile, re-programmable semiconductor memory, i.e., read only memory, (14, figure 1 and col. 4 lines 41-48) comprising partitioning said memory into a plurality of partitions each having a defined address(62, figure 3 and col. 20 lines 56-60), and storing the defined address for one partition in another partition (col. 7 line 45 through col. 8 line 61).

Regarding claim 2, Bunnell discloses a method further including storing information about the number of partitions (col. 6 line 10 through col. 7 line 26).

Regarding claims 3-5, Bunnell discloses a method further including store a boot loader (68, figure 3 and col. 7 lines 53-65), a file system (col. 8 lines 41-56) and a kernel for an operating system (col. 8 lines 21-40) in one of the said partition.

Regarding claim 7-9, Bunnell discloses a method further including storing, in association with the address of a partition, information about the type of information stored in the partition (figure 3), storing information about whether or not the information stored at a given partition is a boot loader, a kernel or a file system, and storing information about the load address for said information in association with said address (col. 7 line 45 through col. 9 line 52).

Regarding claim 10, Bunnell discloses a non-volatile, re-programmable semiconductor memory, i.e., (ROM) read only memory (40, figure 2) comprising a plurality of addressable

partitions (figure 2), including a partition storing an operating system (44', figure 2), and a storage location storing an address for one of said partitions in association with information about the information stored in said partition (col. 6 line 30 through col. 7 line 40).

Regarding claim 11, Bunnell discloses the memory is a FLASH memory (col. 7 lines 45-52).

Regarding claims 12-15, Bunnell discloses the memory wherein one of said partitions stores a basic input/output system (col. 4 lines 49-65), a file system (col. 8 lines 41-57), a kernel for an operating system (col. 8 lines 21-28), and a boot loader (68, figure 3).

Regarding claim 26, Bunnell discloses a processor-based system (10, figure 1) comprising a processor (12, figure 1), a volatile memory, i.e., RAM (40, figure 2) coupled to processor (figure 1), and a re-programmable, non-volatile semiconductor memory, i.e., (ROM) read only memory (42, figure 2) coupled to said processor (col. 4 line 28-48), said semiconductor memory including a plurality of partitions (42, figure 2 and 62, figure 3), one of said partitions storing an operating system (44', figure 2) and another of said partitions storing the addresses of the other partitions in association with information about what is stored in each of said partitions (col. 6 line 30 through col. 7 line 40).

Regarding claims 27, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claims 28-30, the limitations of the claims are rejected as the same reasons set forth in claim 12-15.

(10) Response to Argument

Appellant's arguments filed 5/11/2007 have been fully considered but they are not persuasive.

A. Claims 1-15 and 26-30 are unpatentable over claims 1-8 of Tallam (US 6,948,099) on the grounds of nonstatutory obviousness-type double patenting.

In response to appellant's argument that the recited claim of Tallam patent has nothing to do with storing the defined address for one partition in another partition, it appears that previous final rejection mailed 12/28/2006 clearly pointed out the differences between the recited claim in the current application 10/764,617 and US 6,948,099. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the claimed features of he present Application serial No. 10/764,617 are transparently found in US 6,948,099 with obvious wording variation. For example, claim 1 of US 6,948,099 discloses a memory (read as a non-volatile, reprogrammable semiconductor memory because the claimed language of US 6,948,099, as well as the specification, teaches the memory is a FLASH memory, which is re-programmable, see specification col. 2 lines 28-31) comprising a first portion (read as a partition) storing a primary operation (read as an operating system), a second portion (read as storing location) storing a recovery operating system and instructions adapted to obtain a new operating system from outside said memory (read as an address for one of said partitions in associated with information about the information stored in said partition). Although claim 1 of US 6,948,099 does not specifically teach a plurality of addressable partitions, it is old and notoriously well known in the computer art of memory including a plurality of addressable partitions in order to allow data stored in one of the plurality of addressable partition being called for operation. In

addition, Tallam also teaches memory (14, figure 2) including addressable location (col. 2 line 66 through col. 3 line 2) in order to allow data or information storage in one of the plurality of addressable partitions or locations being called or executed by a processor. Thus, one skill in the art would recognize the memory of Tallam in having addressable partitions. Note the recited claims of Tallam have the similar scope, as well as the similar concept, in comparing with the recited claims in current application. It is therefore the double patenting rejection is valid and proper.

In response to appellant's Declaration under 37 C.F.R. § 1.132 filed 10/4/2006 to show that the material in Tallam application was derive from the inventors Rhoads and Ketrenos, it is noted that the Declaration is not met with requirements because the declarations failed to provide submission of evidence establishing the fact that the patentee, applicant of the published application, or author derived his or her knowledge of the relevant subject matter from applicant (see MPEP 715.01 (c) II). In addition, appellant has failed to provide a satisfactory showing that the relevant portions of the patent originated with or were obtained from the instant applicants and that subject matter is now claims. Furthermore, a statement by the applicants regarding their inventorship in view of patent may not be sufficient where there is evidence to the contrary. In this case, applicant failed to provide the evidence of what material being described in figure 5 of Tallam's patent being invented by inventors Rhoads and Ketrenos. Thus, the declaration is not sufficient.

Moreover, MPEP § 804 clearly states that "a timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or

patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement". A Declaration by one other than the invention to show attribution in accordance with MPEP § 716.01 merely is utilized for overcoming prior art rejection under 35 U.S.C. 102 (a), (e), or (f). Thus, the grounds of nonstatutory obviousness-type double patenting cannot be overcome by Declaration under 37 C.F.R. § 1.132.

B. Claims 1-15 and 26-30 are anticipated under 35 U.S. C. § 102 (e) by Tallam (US 6,948,099).

In response to appellant's Declaration under 37 C.F.R. § 1.132 (Attribution) filed 10/4/2006 to overcome the rejection of claims 1-15 and 26-30, the Declaration was insufficient to overcome the rejection because it failed to provide submission of evidence establishing the fact that the patentee, applicant of the published application, or author derived his or her knowledge of the relevant subject matter from applicant (see MPEP 715.01 (c) II). In accordance with MPEP 715.01 (c) II, "When the unclaimed subject matter of a patent, application publication, or other publication is applicant's own invention, a rejection>, which is not a statutory bar, < on that patent or publication may be removed by submission of evidence establishing the fact that the patentee, applicant of the published application, or author derived his or her knowledge of the relevant subject matter from applicant. Moreover applicant must further show that he or she made the invention upon which the relevant disclosure in the patent, application publication, or other publication is based. In re Mathews, 408 F.2d 1393, 161 USPQ 276 (CCPA 1969); In re Facius, 408 F.2d 1396, 161 USPQ 294 (CCPA 1969)." As further

reviewed the Declaration, the practitioner has provided allegations of facts, which is not considered as evidence. Thus, the Declaration failed to provided enough of evidences to prove which inventor(s) with their invented subject matter, or any of evidence to support the practitioner's statements, for example, the Declaration failed to provide evidence of which material(s) as described in figure 5 of Tallam's patent being invented by inventors Rhoads and Ketrenos. As a result, the attribution or derivation points made in the Declaration are insufficient to overcome the section of 102(e) rejection.

C. Claims 1-15 and 26-30 are anticipated under 35 U.S. C. § 102 (e) by Bunnell (US 5,594,903).

In response to appellant's argument that Bunnell fails to teach the step of storing a defined address for one partition in said memory in another partition in said memory, it is noted that Bunnell clearly teaches a non-volatile, reprogrammable semiconductor memory (62, non-volatile portion in main memory 14 (col. 7 lines 41-51) comprising the steps of partitioning said memory into a plurality of partitions (68-78, figure 3), each having a defined address (col. 7 lines 54-53, i.e., boot loader program beginning at its predefined default address), and storing the defined address for one partition in another partition (col. 11 lines 18-21, i.e., Bunnell teaches the program header (112, figure 4B) located in a first partition (76, figure 4B) providing address of the corresponding code segment (120, figure 4B) located in a second partition (78, figure 4B) such that Bunnell anticipated the claimed limitations of storing the defined address, i.e., address of corresponding code segment, for one partition 78 in another partition 76). Note Bunnell clearly teaches all the claimed limitations as recited in independent claims 1, 10 and 26, as well

as dependent claims 2-9, 11-15 and 27-30. Thus, Bunnell anticipates to unduly broad claimed invention. Therefore, the final rejection should be maintained.

D. Conclusion

For the above reasons, the examiner respectfully submits that the referenced teachings anticipate the subject matter of any of the present claims. Therefore, affirming of all outstanding grounds of rejection and rejecting of all pending claims are respectfully solicited.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Zhuo H. Li

Conferees:

Lynne Browne
Appeal Practice Specialist, TQAS
Technology Center 2100

Shah Sanjiv

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100